In the claims:

1. (previously presented) A color management structure for a panel display, comprising:

a display array unit;

a plurality of gate drivers;

a plurality of source drivers, said plurality of gate drivers and said plurality of source drivers driving said display array unit to display an image; and

a timing sequence control unit, said timing sequence control unit outputting a plurality of signals to said plurality of gate drivers and said plurality of source drivers to drive said display array unit, said timing sequence control unit outputting a clock signal and a digital color management data to said plurality of source drivers.

2. (previously presented) The color management structure of claim 1, wherein said digital color management data is adjustable.

3. (original) The color management structure of claim 1, wherein said panel display is a liquid crystal display.

4. (Previously presented) The color management structure of claim 1, wherein said timing sequence control unit includes:

a timing controller receiving a system input and providing said clock

signal; and

a color management control block, coupled to said timing controller, outputting said digital color management data and said clock signal to said plurality of source drivers, said digital color management data being adjustable.

5. (previously presented) The color management structure of claim 4, wherein said color management control block includes:

a storing unit storing a color management basic data; and

a processing unit receiving said color management basic data and an output of said timing controller and outputting said digital color management data and said clock signal.

6. (previously presented) The color management structure of claim 1, wherein each of said plurality of source drivers includes:

a source drive circuit to drive said display array unit; and

a programmable data interface receiving said digital color management data and said clock signal to parallel output a plurality of color voltage level signals to said source drive circuit.

7. (original) The color management structure of claim 6, wherein said plurality of color voltage level signals includes a plurality of color gamma voltage level data.

8. (previously presented) The color management structure of claim 6, wherein said programmable data interface includes:

an input interface receiving said digital color management data and said clock signal and translating said digital color management data via a data format;

a decoder receiving said translated digital color management data and said clock signal and decoding said translated digital color management data, and outputting a decoded data and a control signal; and

a digital-to-analog converting unit receiving said decoded data, said control signal, and said clock signal, and parallel outputting said plurality of color voltage level signals.

9. (original) The color management structure of claim 8, wherein said input interface converts a serial input signal into a plurality of parallel output signals based on said clock signal.

10. (original) The color management structure of claim 8, wherein said digital-to-analog converting unit includes:

a shift register receiving an output of said decoder;

a latch receiving an output of said shift register and receiving said output of said decoder; and

a plurality of digital-to-analog converters, coupled to said latch, corresponding to said plurality of color voltage level signals respectively.

11.(original) The color management structure of claim 1, wherein said timing sequence control unit is integrated into an application specified integrated circuit (ASIC).

12. (previously presented) A source driver for driving a display array unit of a panel display, said source driver comprising:

a source drive circuit to drive said display array unit; and

a programmable data interface receiving a digital color management data and a clock signal to parallel output a plurality of color voltage level signals to said source drive circuit.

13.(original) The source driver of claim 12, wherein said plurality of color voltage level signals includes a plurality of color gamma voltage level data.

14. (previously presented) The source driver of claim 12, wherein said programmable data interface includes:

an input interface receiving said digital color management data and said clock signal and translating said digital color management data via a data format;

a decoder receiving said translated digital color management data and said clock signal and decoding said translated digital color management data, and outputting a decoded data and a control signal; and

a digital-to-analog converting unit receiving said decoded data, said control signal, and said clock signal, and parallel outputting said plurality of color voltage level signals.

15. (original) The source driver of claim 14, wherein said input interface converts a serial input signal into a plurality of parallel output signals based on said clock signal.

16. (original) The source driver of claim 14, wherein said digital-to-analog converting unit includes:

a shift register receiving an output of said decoder;

a latch receiving an output of said shift register and receiving said output of said decoder; and

a plurality of digital-to-analog converters, coupled to said latch, corresponding to said plurality of color voltage level signals respectively.

17. (previously presented) A color management structure for a panel display, comprising:

a display array unit;

a plurality of gate drivers;

a plurality of source drivers, said plurality of gate drivers and said plurality of source drivers driving said display array unit to display an image;

a timing sequence control unit, said timing sequence control unit

outputting a plurality of signals to said plurality of gate drivers and said plurality of source drivers to drive said display array unit, said timing sequence control unit outputting a clock signal; and

a color management interface system, coupled to said timing sequence control unit and said plurality of source drivers, generating a digital color management data to said plurality of source drivers.

18. (original) The color management structure of claim 17, wherein said color management interface system includes a color management control block in said timing sequence control unit and a color data converting unit in each of said plurality of source drivers to obtain a plurality of color voltage level signals for said plurality of source drivers.

19. (previously presented) A panel display comprising:

a display array unit;

a plurality of drivers driving said display array unit to display an image; and

a timing sequence control unit, said timing sequence control unit outputting a plurality of signals to said plurality of drivers to drive said display array unit, said timing sequence control unit outputting a clock signal and a digital color management data to said plurality of drivers.

20. (previously presented) The panel display of claim 19, wherein said

digital color management data is a serial color management correction data.

21. (cancelled)